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EXAMINER	
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ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	09/932,086	FARKAS ET AL.	
	Examiner	Art Unit	
	Guy J. Lamarre	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2008*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,4,5 and 10-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4,5 and 10-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

GENERAL OFFICE ACTION

* **Claims 2, 4-5, 10-19** remain pending.

1. The prior art rejections of record are maintained in response to Applicants' Amendment.

Response to Arguments

Applicants' arguments of 12/12/2007 have been fully considered, but are not persuasive.

REMARKS

.1 In response to **Claims 2, 4-5** and **10-19,** Applicants argue that the prior art of record does not teach logic testing because **Osawa et al.** (US Pat. 5946247) and **Satoh** (US Pat. # 6477672; filed 21 Sept. 1999) are directed exclusively to memory testing.

Examiner disagrees and notes that **Osawa,** at col**.** 41 line 37, performs logic test or functional test of the memory.

For Example:

Applicant is directed to **Osawa** at col. 1 line 10 which states: '***The present invention relates to a <u>testing device for making a functional test on a semiconductor memory</u> which <u>is a logic integrated circuit</u> including a plurality of RAMs, a plurality of ROMS and the like***.'

Examiner also notes that even Applicant concedes at page 5 of the response that '' the testing of logic can require a much larger and more complex set of test vectors than needed to test memories due to the different nature of the faults that are likely to occur. **In the past, testing of logic has required either a large test vector memory external to the IC** (increasing test system complexity and cost) **or a test vector generator integrated directly into the IC** (increasing chip design considerations and chip area, and hence chip costs). Testing of memories

involves generating much smaller sets of simple test vectors, thus not presenting the problems solved by Applicant's claimed invention."

.2 Applicants also argue that the prior art of record does not teach '**programming the programmable test vector generator to provide pseudo-random test…**' Examiner disagrees.

For Example:

Applicant is directed to **Osawa**'s col. 75 line 30 et seq. 'The self test circuit 702 includes a microcomputer 702a as shown in FIG. 143. A ***<u>program stored in a ROM or a RAM (not shown) of the microcomputer 702a controls a self test operation</u>***. Since it is possible to supply a test result to the microcomputer 702a and transmit to the entire system (e.g., a system of upper hierarchy) through an input/output port of the microcomputer 702a, it is possible that the upper hierarchy system recognizes a failure, and hence, it is possible to maintain the upper hierarchy system in an easy manner. For example, when there are too many failures for the redundancy circuit 704 to compensate, the upper hierarchy system can recognize this and stop the system operation. In FIG. 143, the reset signal from the power on reset circuit 701 is indicated as "Reset Signal," **<u>a test pattern signal supplied to the RAM with test circuit 703 is indicated as "Test Pattern"</u>** and a register control signal supplied to the register circuit 706 is indicated as "Register Control."

Applicant is also directed to **Osawa**'s col. 89 line 5 et seq. 'In the circuit shown in FIG. 124 or 125, however, test address terminals TA (TA0, TA1, TA2, . . .) are selected when a CHDIR signal is set at "1", dissimilarly to that shown in FIG. 93 or 94. As shown in FIG. 121, the test address terminal TA is provided as a RAMK pin. Therefore, it is possible to set addresses in arbitrary order to make a test. Namely, B-SCAN can set addresses by a serial shift

operation when the CHDIR signal is "0". When the CHDIR signal is "1", on the other hand, it is possible to set addresses in a parallel manner by the test address terminal TA. **An address signal for the test address terminal TA may be supplied from an external pin of an LSI, or by a test address generation circuit (corresponding to 301 in FIG. 60) which is built in the interior of the LSI.** This **test address generation circuit may be prepared from an algorithmic pattern generator which is provided in a memory LSI test device'**

.3 In regards to **Claims 2, 4-5** and **10-19** as rejected under 35 U.S.C. 103(a) over **Abramovici and Osawa,** Applicants also argue that the prior art of record '*does not appear to disclose an external tester that includes a programmable test vector generator for testing logic circuitry***.**' Examiner disagrees.

Applicant is also directed to **Osawa**'s col. 89 line 5 et seq. 'In the circuit shown in FIG. 124 or 125, however, test address terminals TA (TA0, TA1, TA2, . . .) are selected when a CHDIR signal is set at "1", dissimilarly to that shown in FIG. 93 or 94. As shown in FIG. 121, the test address terminal TA is provided as a RAMK pin. Therefore, it is possible to set addresses in arbitrary order to make a test. Namely, B-SCAN can set addresses by a serial shift operation when the CHDIR signal is "0". When the CHDIR signal is "1", on the other hand, it is possible to set addresses in a parallel manner by the test address terminal TA. **An address signal for the test address terminal TA may be supplied from an external pin of an LSI, or by a test address generation circuit (corresponding to 301 in FIG. 60) which is built in the interior of the LSI.** This **test address generation circuit may be prepared from an algorithmic pattern generator which is provided in a memory LSI test device'**

In regards to **Claims 2, 4-5** and **10-14** as rejected under 35 U.S.C. 103(a) over **Abramovici and Osawa,** Applicants further argue that the prior art of record does not ' *teach or suggest programming the programmable test vector generator to provide pseudo-random test vectors and deterministic test vectors to the logic circuitry under test, to provide test vectors in real time to the logic circuitry under test, or to modify the test vectors based on the logic circuitry to be tested…'*

Examiner disagrees and directs Applicant to **Osawa**'s col. 89 line 5 et seq., e.g., 'In the circuit shown in FIG. 124 or 125, however, test address terminals TA (TA0, TA1, TA2, . . .) are selected when a CHDIR signal is set at "1", dissimilarly to that shown in FIG. 93 or 94. As shown in FIG. 121, the test address terminal TA is provided as a RAMK pin. Therefore, it is possible to set addresses in arbitrary order to make a test. Namely, B-SCAN can set addresses by a serial shift operation when the CHDIR signal is "0". When the CHDIR signal is "1", on the other hand, it is possible to set addresses in a parallel manner by the test address terminal TA. **An address signal for the test address terminal TA may be supplied from an <u>external pin of an LSI</u>, or by a test address generation circuit (corresponding to 301 in FIG. 60) which is built <u>in the interior of the LSI</u>.** This **<u>test address generation circuit may be prepared from an algorithmic pattern generator which is provided in a memory LSI test device'</u>**

In regards to Applinat's comments:' *programmable test vector generator to provide pseudo-random test vectors and deterministic test vectors to the logic circuitry under test, to provide test vectors in real time to the logic circuitry under test, or to modify the test vectors based on the logic circuitry to be tested.'*

Examiner does not understand why Applicant fail to realize that testing requires *pseudo-random test vectors and deterministic test vectors as s*timuli.

Examiner maintains that the prior art is clear in **Osawa**'s col. 89 line 5 et seq., which states that: '*This* ***test address generation circuit may be prepared from an algorithmic pattern generator which is provided in a memory LSI test device'***

Claim Rejections - 35 USC ' 102

2. **Claims 2, 4-5** and **10-19 (is)** are rejected under 35 U.S.C. 102 (b) as being anticipated by **Osawa et al.** (US Pat. 5946247).

As per Claim 10, Osawa et al. discloses an –interior/exterior- tester/testing device for testing logic circuitry or functional testing of an integrated circuit –Fig. 25 and col. 40 line 48-col. 41 line 46-, comprising a **programmable** test vector/pattern generator- col. 41 line 37-for generating test vectors/patterns for the logic circuitry or functional test of the memory.

As per Claim 5, Osawa et al. discloses tester of claim 10, wherein the programmable test vector generator is a programmable algorithmic test vector generator which includes an arithmetic and logic unit and generates test vectors in real time in Figs. 25-26 and col. 41 line 34.

2.1 **Claim 4 (is)** are rejected under 35 U.S.C. 102 (b) as being anticipated by **Osawa et al.** (US Pat. 5946247) or under 35 U.S.C. 103(a) in the alternative.

As per Claim 4, **Osawa et al.** discloses tester of claim 10, comprising a test response analysis unit arranged to compress test response vectors received from the integrated circuit to be tested. -*FIG. 132 shows a semiconductor memory testing device according to fourth prior art. Semiconductor memories (RAM 1, RAM 2 and RAM 3) shown in FIG. 132 have data output scan*

paths DO (scan FFs provided with data compression functions) respectively, so that an output from the scan path DO of a preceding semiconductor memory is inputted in that of a subsequent semiconductor memory. Test results are made by shift operations of the respective scan paths DO. In order to compress data for testing with respect to the respective semiconductor memories, SINH signals (shift inhibiting signals) are inputted to inhibit shift operations of the scan paths DO.-

In the alternative, compressing/compacting test result data, e.g., via a MISR or shift register, is obvious for optimizing memory storage of such test result data.

As per Claims 2, 11, said claims do not depart in scope or spirit from the teachings of **Osawa,** and thus stand rejected on the same rationale as the rejection of Claims 4-5, 10.

As per Claims 12-19, said claims do not depart in scope or spirit from the teachings of **Osawa**, and thus stand rejected on the same rationale as the rejection of Claims 5, 10.

2.2 **Claims 2, 4-5** and **10-19 (is)** are rejected under 35 U.S.C. 102 (e) as being anticipated by **Satoh** (US Pat. # 6477672; filed 21 Sept. 1999).

As per Claim 10, Satoh discloses an –interior/exterior- tester/testing device for testing logic circuitry or functional testing of an integrated circuit –Fig. 1 and related description, comprising a **programmable** test vector/pattern generator- Abstract-for generating test vectors/patterns for the logic circuitry, e.g., '*A pattern generating sequence described in the test program stored in the main controller 100 is previously stored in the pattern generator TG prior to the start of a test. When a test start instruction is given thereto from the main controller 100, the pattern generator PG outputs test pattern data to be applied to the memory under test MUT in accordance with the stored pattern generating sequence. As the pattern generator PG, an ALPG*

(Algorithmic Pattern Generator) is generally used. The ALPG is a pattern generator that generates a test pattern to be applied to a semiconductor device (for example, an IC) by an arithmetic and logic operation or computation using internal registers each having an arithmetic and logic function or computing function.'

As per Claim 5, Satoh discloses tester of claim 10, wherein the programmable test vector generator is a programmable algorithmic test vector generator which includes an arithmetic and logic unit and generates test vectors in real time in Fig.1 and Abstract.

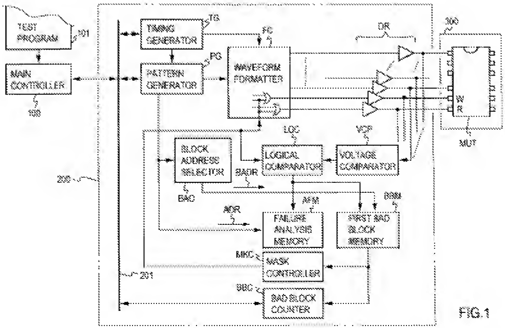


FIG.1

As per Claims 2, 11, said claims do not depart in scope or spirit from the teachings of **Satoh.,** and thus stand rejected on the same rationale as the rejection of Claims 5, 10.

As per Claims 12-19, said claims do not depart in scope or spirit from the teachings of **Satoh.,** and thus stand rejected on the same rationale as the rejection of Claims 5, 10.

Claim Rejections - 35 USC ' 103

3. **Claims 2, 4-5** and **10-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over as being unpatentable over **Abramovici et al.** and **Osawa et al.** (US Pat. # 5946247)

As per Claims 2, 4-5 and **10-19, Osawa et al.** substantially discloses, e.g., in Fig. 25, a *tester/testing device* that generates logic/functional test patterns/vectors to test/diagnose the logic circuitry of semiconductor memory 3*1* to enable fault localization.

Not specifically described in detail in **Osawa et al.** is the approach whereby tester is of programmable test generation type.

However Abramovici et al., in an analogous art, discloses *"Digital Systems testing and Testable Design,"* wherein such techniques are described. {See **Abramovici et al.,** Id., Pgs. 479-487, wherein, e.g., shift registers are programmed (or PRPG: at page 483) via seed values to generate test patterns/sequences for test application thereof to the device under test.}

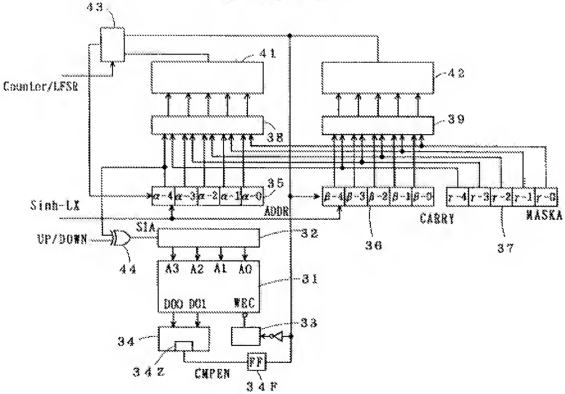
Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in **Osawa et al.** by including therein programmable test pattern circuitry for external application of test data as taught by **Abramovici et al,** because such modification would provide the procedure disclosed in **Osawa et al.** with a technique whereby *"TPG (test pattern generation) is external to the semiconductor and hence not part of the functional circuitry. ..."* to also thereby reduce tester hardware overhead. {See **Abramovici et al,** page 481 : last sentence.}

Abramovici et al. discloses equivalent test sequencing/output response analysis/ compression (e.g., via MISR: at page 483) , e.g., on pages 477, 481, and 483.

As per Claim 5, Osawa et al. discloses, e.g., in Fig. 25 and related description at col. 40 line 48-col. 41 line 46, that the test patterns/test vectors are generated via a processor or an

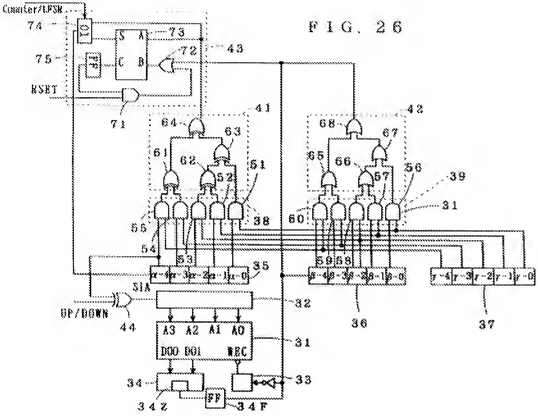
arithmetic and logic structure/ ALU wherein detailed component layout for the ALU is shown in Fig. 26 and disclosed in col. 41 line 47 et seq., e.g., '*FIG. 25 illustrates the semiconductor memory testing device*

FIG. 25



according to the fourth embodiment of the present invention. The semiconductor memory testing device according to this embodiment is a 5-bit address generation circuit which generates pseudo-random series within 5 bits while enabling count up/down, for making a functional test on a plurality of semiconductor memories (tested circuits) such as RAMs or ROMs while generating 5-bit addressing data as pseudo-random numbers. Referring to FIG. 25, numeral 31 denotes a tested circuit (semiconductor memory) such as a RAM whose word number (address input terminal number) is set at an arbitrary value such as 2.sup.4, for example,

FIG. 26



numeral 32 denotes a 4-bit address input shift register for inputting addresses in address input terminals A0 to A3 of the tested circuit 31, numeral 33 denotes a data input register serving as a write enable (write control) command part, numeral 34 denotes a 2-bit comparison circuit (data output shift register) for comparing data output values of the RAM with an expected value, numeral 35 denotes a 5-bit address generation shift register (address generation part: ADDR) storing initial values of RAM addresses, symbols .alpha.-0 (least significant bit: LSB) to .alpha.-4 (most significant bit: MSB) denote flip-flops (1-bit registers) forming the address generation shift register (ADDR) 35, numeral 36 denotes a 5-bit control register (CARRY), symbols .beta.-0 (least significant bit: LSB) to .beta.-4 (most significant bit: MSB) denote flip-flops (1-bit registers) forming the control register (CARRY) 36, numeral 37 denotes a 5-bit flip-

flop selection register (effective address number storage part: MASKA) receiving generating functions of all cyclic series as initial values in addressing and storing an effective address number in counting, symbols .gamma.-0 (least significant bit: LSB) to .gamma.-4 (most significant bit: MSB) denote flip-flops forming the flip-flop selection register (MASKA) 37, numeral 38 denotes a first AND (logical product) circuit group obtaining logical products (AND) between the flip-flops .alpha.-0 to .alpha.-4 of the address generation shift register (ADDR) 35 and the flip-flops .gamma.-0 to .gamma.-4 of the flip-flop selection register (MASKA) 37 corresponding thereto respectively, numeral 39 denotes a second AND (logical product) circuit group obtaining logical products (AND) between the flip-flops .beta.-0 to .beta.-4 of the control register (CARRY) 36 and the flip-flops .gamma.-0 to .gamma.-4 of the flip-flop selection register (MASKA) 37 corresponding thereto respectively, numeral 41 denotes an expected value generation circuit, numeral 42 denotes an OR (logical sum) circuit group for obtaining a logical sum (OR) for the output of the second AND circuit 39, numeral 43 denotes a counter, and numeral 44 denotes an exclusive OR (Ex.OR) circuit. The address generation shift register (ADDR) 35, the control register (CARRY) 36, the flip-flop selection register (MASKA) 37, the first AND circuit group 38, the second AND circuit group 39, the expected value generation circuit 41, and the OR circuit group 42 form an arithmetic and logic part which generates a test pattern of a bit number corresponding to the maximum address value of addresses of a plurality of types of semiconductor memories subjected to a functional test in test pattern generation, while setting effective address numbers of the semiconductor memories in counting.'

Claim Rejections - 35 USC ' 101

* 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

.1 **Claim 10** and **intervening claims are** rejected under 35 U.S.C. 101 as being devoid of a useful tangible result.

Examiner notes that a tester needs circuitry:

to apply test stimuli to a circuit,

to compare circuit response to same stimuli with expected response and

to provide a determination as to whether same circuit is errorfree.

Claim Rejections - 35 USC § 112

* The following is a quotation of the first and **second** paragraphs of 35 U.S.C. 112:

> 1. The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
>
> 2. The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

.1. **Claim 10** and **intervening claims are** rejected under the **first paragraph of 35 U.S.C. 112** for failing to describe the manner in which the tester effects testing without stimulus application to circuit under test.

.2. Claim 10 and **intervening claims** are rejected under the second paragraph of 35 U.S.C. 112 as being indefinite and as missing essential structural elements. It is unclear to the Examiner what component limitation is being claimed and how the tester effects testing.

Conclusion

* Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached at (571) 272-6962.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Guy J Lamarre/

Primary Examiner, Art Unit 2112